DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Regular End Semester Examination – Summer 2022

Course: T.Y.B. Tech. **Semester: VI**

Subject Code & Name: Digital System Design (BTETOE605A)

Max Marks: 60 **Date: 20/08/2022** **Duration: 3.45 Hr.**

Instructions to the Students:

1. *All the questions are compulsory.*
2. *The level of question/expected answer as per OBE or the Course Outcome (CO) on which the question is based is mentioned in ( ) in front of the question.*
3. *Calculators is not allowed.*

(Level/CO) Marks

Q. 1 Solve Any Two of the following.

A) Convert the following expression in standard SOP form **06**
$F=A+B'C$

B) Implement full adder and full subtractor using decoder and OR gates. **06**

C) What is State diagram? Explain in detail state table and excitation tables with suitable example **06**

Q.2 Solve Any Two of the following.

A) Derive characteristic equations for J-K, D and T F/Fs **06**

B) Draw Universal shift Register with following operations. **06**

Control or select line	Operation
11	Parallel load
10	Shift left
01	Shift right
00	No operation

C) What is difference between TTL and CMOS. **06**

Q. 3 Solve Any Two of the following.

A) Solve the following example using 4-variable K-map **06**
$F=\sum m\ (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$

B) Design logic circuit to convert 3-bit Binary code into a Gray code **06**

C) Draw clock waveform (timing diagram) for BCD twisted counter. **06**

Q. 4 Solve Any Two of the following.

A) Design 3 bit synchronous sequential counter using T flipflop. **06**

B) Define following terms. **06**
i) Propagation delay ii) rise time iii) Fall time
iv) delay time v) fan-in vi) fan-out

C) Implement 5 to 32 decoder using only 3 to 8 decoders. **06**

Q. 5 Solve Any Two of the following.

A) How many types of memory are there in digital electronics? **06**

B) Write VHDL code for 4x1 MUX using dataflow and behavioral architecture style. **06**

C) Explain FPGA architecture with suitable diagram. **06**

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