DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Supplementary End Semester Examination – Summer 2022

Course: B. Tech.   **Branch: EXTC**   **Semester : VII**

Subject Code & Name: BTETPE703C (VLSI Design & Technology)

Max Marks: 60   **Date:22/08/2022**   **Duration: 3.45 Hr.**

Instructions to the Students:
1. *All the questions are compulsory.*
2. *The level of question/expected answer as per OBE or the Course Outcome (CO) on which the question is based is mentioned in ( ) in front of the question.*
3. *Use of non-programmable scientific calculators is allowed.*
4. *Assume suitable data wherever necessary and mention it clearly.*

		(Level/CO)	Marks

Q. 1 Solve Any Two of the following.

A) Implement following Boolean function using PROM, PLA and PAL.   **6**

$$A(X,Y,Z)=\sum m(5,6,7)$$
$$B(X,Y,Z)=\sum m(3,5,6,7)$$

B) What is interconnect in SoC?   **6**

C) What is JTAG based boundary scan testing?   **6**

Q.2 Solve Any Two of the following.

A) Explain CMOS common Gate amplifier.   **6**

B) Write VHDL code for 4x1 mux using Concurrent and sequential statements.   **6**

C) Explain LUT used in FPGA architecture?   **6**

Q. 3 Solve Any Two of the following.

A) Difference between CPLD and FPGA.   **6**

B) What is the need of DFT in VLSI?   **6**

C) Draw and explain DC transfer characteristics of CMOS inverter.   **6**

Q.4 Solve Any One of the following.

A) What are the different types of architectures used in the VHDL? Explain with Half adder as an example.   **12**

B) Draw Layout diagram of NAND gate with all dimensions.   **12**

Q. 5 Solve Any Two of the following.

A) Draw the CMOS AND and NOR gate.   **6**

What is the technological reason for using universal gate for design?

B) What is the difference between Signal and Variable in VHDL   **6**

C) Explain Small signal equivalent analysis of MOS Differential Amplifier.   **6**

*** End ***