DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Summer End Semester Examination –2022

Course: M. Tech.   **Semester : II**

Subject Code & Name: MTECE244C (Digital VLSI Design)

Max Marks: 60   **Date:20/10/2022**   **Duration: 3.00 Hr.**

Instructions to the Students:
1. *All the questions are compulsory.*
2. *The level of question/expected answer as per OBE or the Course Outcome (CO) on which the question is based is mentioned in ( ) in front of the question.*
3. *Use of non-programmable scientific calculators is allowed.*
4. *Assume suitable data wherever necessary and mention it clearly.*

	Marks

Q. 1 Solve Any Two of the following. **(12)**

A) Write VHDL code for 4x1 mux using Concurrent and sequential statements.

B) Which memory is better: SRAM or DRAM? Explain.

C) Explain LUT used in FPGA architecture?

Q.2 Solve Any Two of the following. **(12)**

A) Draw and explain DC transfer characteristics of CMOS inverter.

B) Difference between CPLD and FPGA.

C) What is floorplanning and placement in VLSI circuits?

Q. 3 Solve Any Two of the following. **(12)**

A) Draw the CMOS schematic diagram for :AND gate and NOR gate

What is the technological reason for using universal gate for digital design?

B) What is the need of DFT in VLSI?

C) What is 6T SRAM cell?

Q.4 Solve Any one of the following. **(12)**

A) Write VHDL code for given equation using dataflow, structural and Behavioral architecture style.

$y = \sum m (1,2,4,7)$

B) Draw CMOS Layout for y= (AB + CD)'.

Write layout names and dimensions properly.

Q. 5 Solve Any Two of the following. **(12)**

A) What are stuck at 0 and stuck at 1 fault?

B) What is the difference between Signal and Variable in VHDL

C) Implement following Boolean function using PROM, PLA and PAL.

$A(X,Y,Z)=\sum m(5,6,7)$

$B(X,Y,Z)=\sum m(3,5,6,7)$

*** End ***